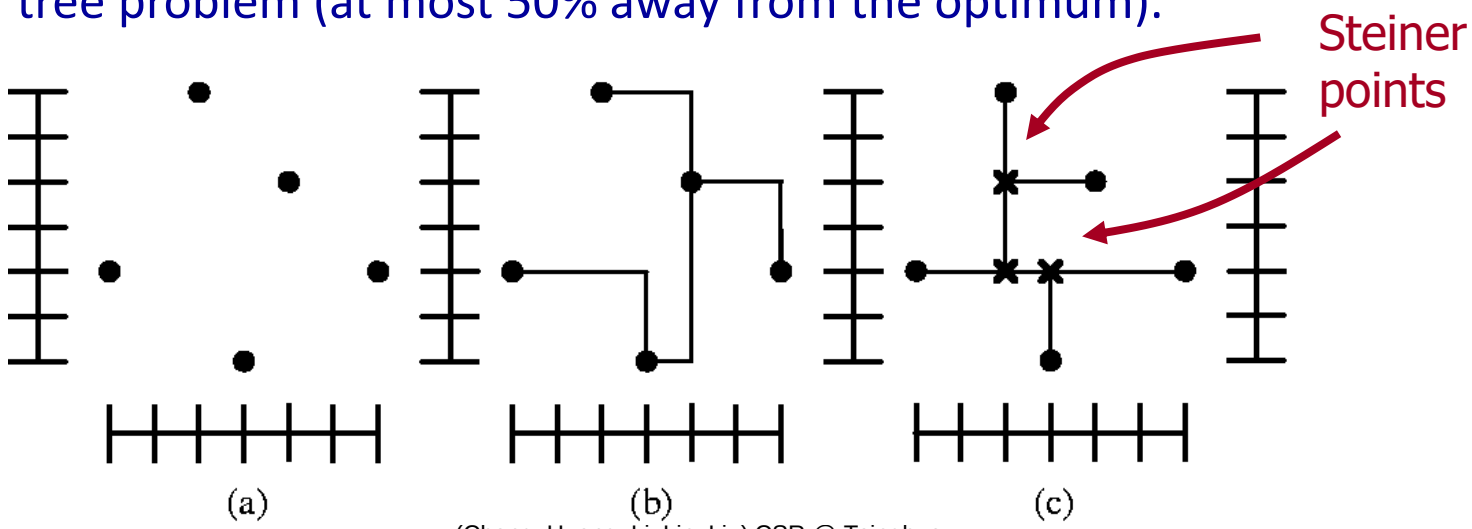
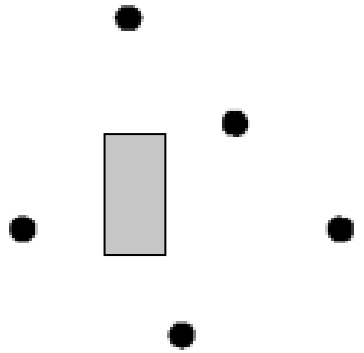
Spanning Tree v.s. Steiner Tree

- **Manhattan distance:** If two points (nodes) are located at coordinates (x_1, y_1) and (x_2, y_2), the Manhattan distance between them is given by $d_{12} = |x_1-x_2| + |y_1-y_2|$.
- **Rectilinear spanning tree:** a spanning tree that connects its nodes using Manhattan paths (Fig. (b) below).
- **Steiner tree:** a tree that connects its nodes, and additional points (**Steiner points**) are permitted to used for the connections.
- The minimum rectilinear spanning tree problem is in P, while the minimum rectilinear Steiner tree (Fig. (c)) problem is NP-complete.
  - The spanning tree algorithm can be an *approximation* for the Steiner tree problem (at most 50% away from the optimum).



What if there is a blockage?



https://vlsicad.ucsd.edu/GSRC/bookshelf/Slots/RSMT/RMST/

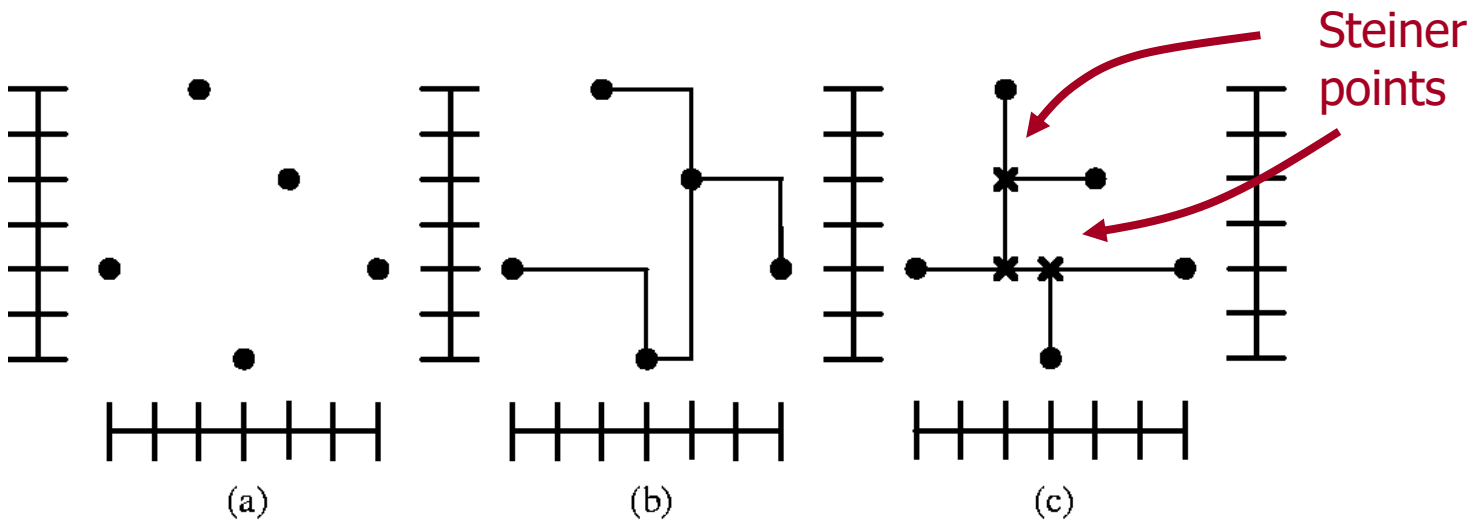
RMST-Pack: Rectilinear Minimum Spanning Tree Algorithms

https://github.com/shininglion/rectilinear_spanning_graph

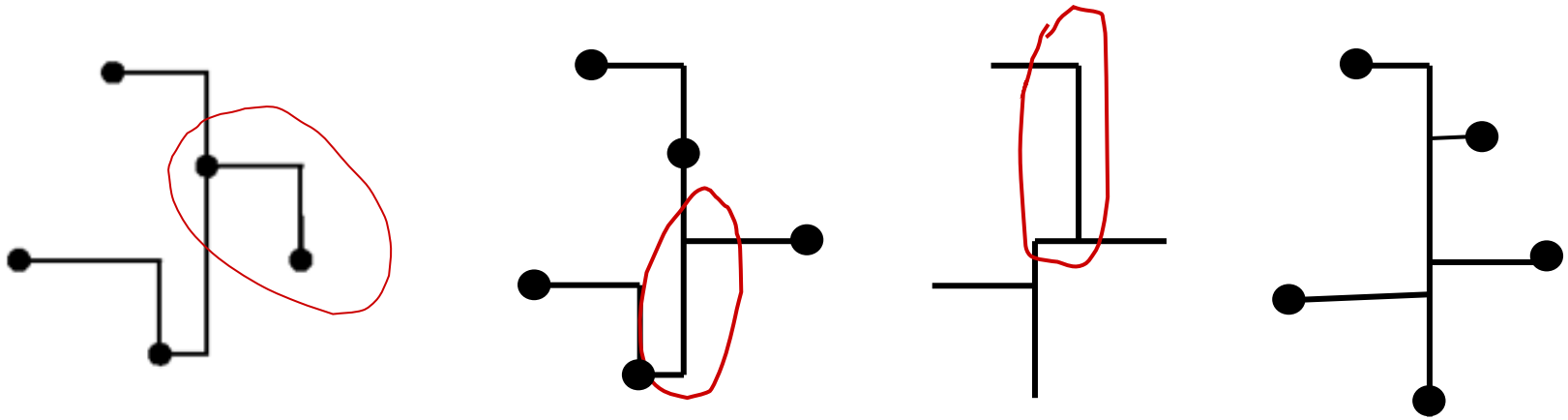
This library contains rectilinear spanning graph construction, finding minimum spanning tree and an implementation of binary search tree

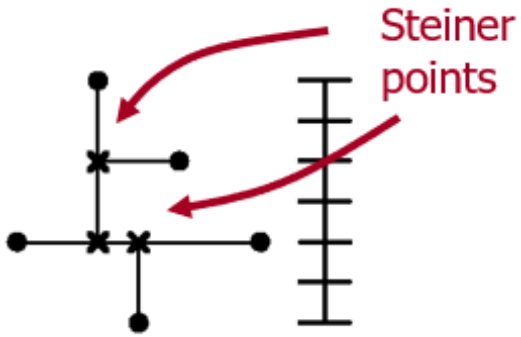
https://home.engineering.iastate.edu/~cnchu/flute.html
FLUTE: Fast Lookup Table Based Technique for RectSteiMinTree Construction and Wirelength Estimation

https://vlsicad.ucsd.edu/Publications/Conferences/355/c355.pdf
Prim-Dijkstra Revisited: Achieving Superior Timing-driven Routing Trees
•Charles J. Alpert, Wing-Kai Chow, Kwangsoo Han, Andrew B. Kahng, Zhuo Li 0001, Derong Liu, Sriram Venkatesh. 10-17 [doi]
ISPD 2018



How To Transform Into Rectilinear Min Steiner Tree





Can we improve more?

More complications, such as
(1) blockages (2) layer changes

More Geometry Variations

- Previously we talk about wiring in Manhattan style
- For flat panel & packaging, we can see many different wiring styles

Just A Preview – Different Kind Of Routing

Any angle wiring, rubber banding, piecewise linear wiring

United States Patent
Chang et al.

(10) **Patent No.: US 8,875,083 B2**
(45) **Date of Patent: Oct. 28, 2014**

ROUTING METHOD FOR FLIP CHIP PACKAGE AND APPARATUS USING THE SAME

2924/014 (2013.01); *H01L 2224/14136* (2013.01); *H01L 24/14* (2013.01); *H01L*

(Continued)

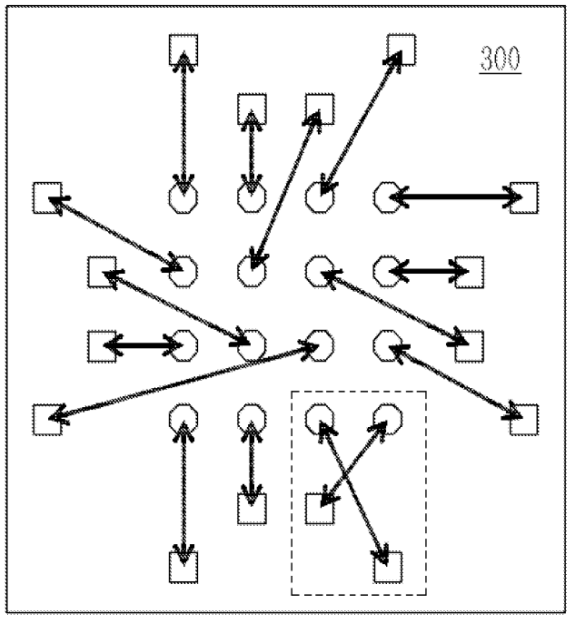


FIG. 3

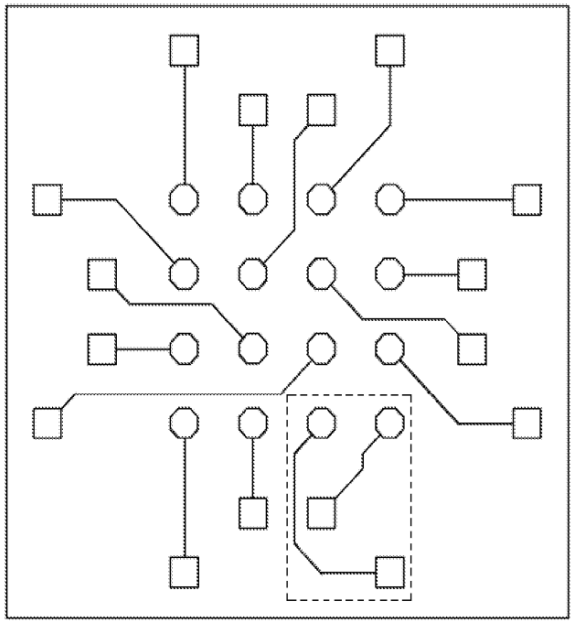


FIG. 4

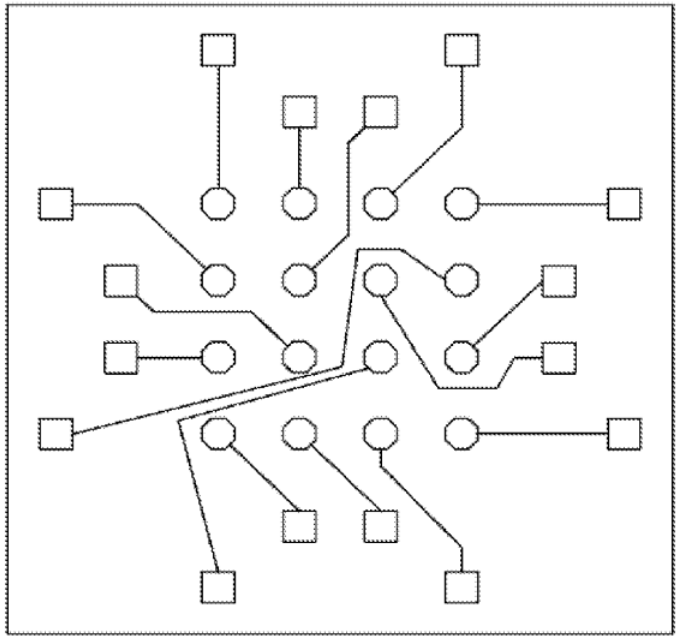
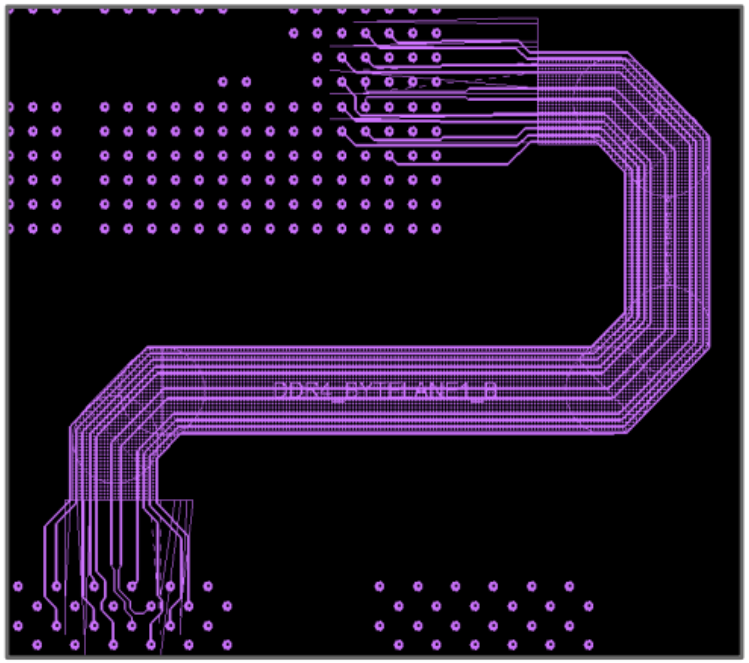


FIG. 23

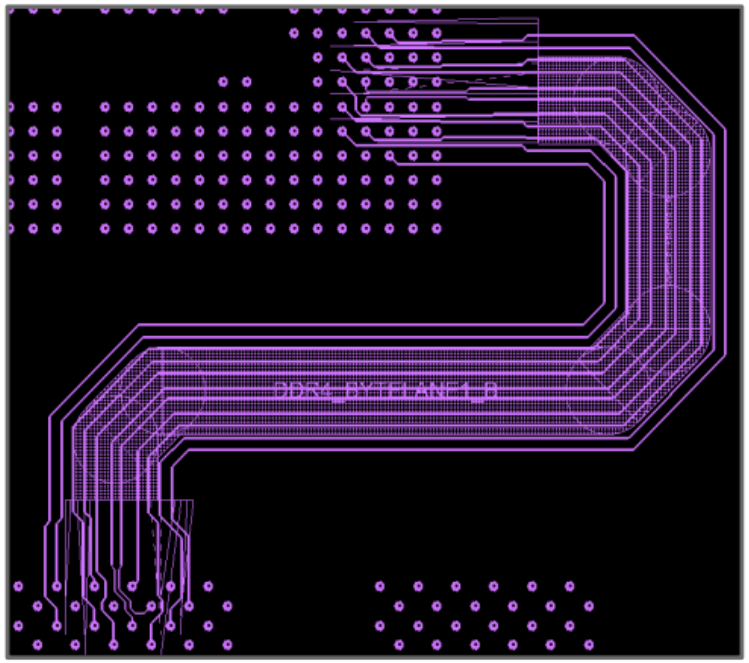
Trunk Route of Escape Routing

Complete following recommended routing flow

- Breakout has been completed on both ends of bundle so a direct route “trunk route” can be made to complete connections



- Trunk route uses minimum DRC spacing and can be easily re-spaced using a user-defined value for a larger spacing margin



CAD Related Conferences/Journals

- Important Conferences:
  - **ACM/IEEE Design Automation Conference (DAC)**
  - **IEEE/ACM Int'l Conference on Computer-Aided Design (ICCAD)**
  - ACM/IEEE Asia and South Pacific Design Automation Conf. (ASP-DAC)
  - ACM/IEEE Design, Automation, and Test in Europe (DATE)
  - IEEE Int'l Conference on Computer Design (ICCD)
  - IEEE Custom Integrated Circuits Conference (CICC)
  - IEEE Int'l Symposium on Circuits and Systems (ISCAS)
  - **ACM Int'l Symposium on Physical Design (ISPD)**
  - IEEE Int'l Test Conference (ITC)
  - Others: VLSI Design/CAD Symposium/Taiwan
- Important Journals:
  - **IEEE Transactions on Computer-Aided Design (TCAD)**
  - **ACM Transactions on Design Automation of Electronic Systems (TODAES)**
  - **IEEE Transactions on VLSI Systems (TVLSI)**
  - **IEEE Transactions on Computers (TC)**
  - IEE Proceedings – Circuits, Devices and Systems
  - IEE Proceedings – Digital Systems
  - INTEGRATION: The VLSI Journal

Summary So Far

- Algorithm types (P, NP, NP-Complete, NP-Hard, …)
- Travelling salesman problem
- Minimum spanning tree
- Minimum Steiner tree
- Hamiltonian circuit
- Circuit-Satisfiability Problem (SAT)
- Search, dynamic programming
- Bin packing
- Minimum rectilinear Steiner tree

Steiner tree (and min spanning tree) very useful in layout.
SAT useful in logic synthesis, formal verification.

Lately we saw

TSMC N2 Design Flow Certification: https://bit.ly/3rsT5Gp
Analog Design Migration Advancements: https://bit.ly/46v4FzL
Automotive-Grade IP for N5A Process: https://bit.ly/3EQrGRU
Multi-Die System Design Advancements: https://bit.ly/3EYM7vK